Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1. (Currently Amended) A method of developing an ASIC comprising:

developing a hardware model including a CPU bus functional model, and a software coupled to a CPU server concurrently;

communicating command and control information between the CPU server and the CPU bus functional model over a network **according to an XBUS protocol**;

co-simulating the hardware model and the software; and

receiving real working environment test inputs for the co-simulation.

Claim 2. (Previously Presented) The method of claim 1, wherein the hardware model is developed on a workstation.

Claim 3. (Original) The method of claim 1, wherein the software is developed on a target board.

Claim 4. (Canceled)

Claim 5. (Previously Presented) The method of claim 1, wherein the co-simulated hardware model is described by a high-level language model.

Claim 6. (Canceled)

Claim 7. (Canceled)

Claim 8. (Currently Amended) A method of co-simulating a hardware model and a software in ASIC development, comprising:

Requesting**, by a hardware side including a CPU bus functional model,** ~~an~~ access to ~~the hardware model including a CPU bus functional model from a hardware component to~~ a software ~~component coupled to~~ **side, including** a CPU server**,** over a network **according to an XBUS protocol**;

invoking a function call by the CPU server;

sending an access request from the CPU bus functional model to the CPU server over the network **according to the XBUS protocol**;

routing the access request to the hardware model;

co-simulating the hardware model and the software; and

receiving real working environment test inputs for the co-simulation.

Claim 9. (Original) the method of claim 8, wherein the function call is a READ function call.

Claim 10. (Original) The method of claim 8, wherein the function call is a WRITE function call.

Claim 11. (Previously Presented) The method of claim 8, further comprising:

requesting a hardware model interrupt; and

handling the hardware model interrupt with a function call invoked by the software component over the network.

Claim 12. (Currently Amended) An apparatus for hardware model and software co-simulation in ASIC development, comprising:

a hardware model including a CPU bus functional model to represent a hardware board circuit;

a software **coupled to a CPU server** to provide command and control access of the hardware model; **and**

~~**a target board including a CPU server in communication with the software; and**~~

a network coupled to the CPU bus functional model and the CPU server to communicate a command from the software to the hardware model and to route contents of the command between the hardware model and software **according to an XBUS protocol** to provide co-simulation of the hardware model and software

wherein the hardware model is configured to receive real working environment test inputs for the co-simulation.

Claim 13. (Canceled)

Claim 14. (Currently Amended) The apparatus of claim ~~13~~ **12**, wherein the software is loaded on the CPU server.

Claim 15. (Canceled)

Claim 16. (Canceled)

Claim 17. (Canceled)

Claim 18. (New) The method of developing the ASIC of claim 1 further comprising the hardware model and the software communicating according to the XBUS protocol exchanging data without a physical bus.

Claim 19. (New) The method of developing the ASIC of claim 18 further comprising:

sharing, by all modules of the hardware model and the software communicating according to the XBUS protocol, a plurality of registers.

Claim 20. (New) The method of co-simulating the hardware model and the software in ASIC development of claim 8 further comprising the hardware model and the software communicating according to the XBUS protocol exchanging data without a physical bus.

Claim 21. (New) The method of co-simulating the hardware model and the software in ASIC development of claim 20 further comprising:

sharing, by all modules of the hardware model and the software communicating according to the XBUS protocol, a plurality of registers.

Claim 22. (New) The apparatus for hardware model and software co-simulation in ASIC development of claim 12 wherein the hardware model and the software communicating according to the XBUS protocol are configured to exchange data without a physical bus.

Claim 23. (New) The apparatus for hardware model and software co-simulation in ASIC development of claim 22 further comprising a plurality of shared registers coupled to the hardware model and the software configured to communicate according to the XBUS protocol.